ISSN 2229-5518

A Comparative Analysis of conventional inverter with multilevel inverter - a simulation study

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ABSTRACT—Advances in power electronics technology allowed the wide investigation of multilevel inverters that provide high safety voltages with less harmonic components as compared to the conventional two-level structures. In this paper multi-level inverter topology Diode clamped multi-level inverter (DCMLI) and conventional inverter (180 ^{0} and 120 ^{0}) are considered for comparative analysis. The comparative analysis is carried out in terms of THD of output voltage. A pulse width modulation (PWM) based switching technique is employed for the switching of Insulated Gate Bipolar Transistors (IGBTs) of the inverters. Moreover, operating principle, features, parameters and potential application of these inverters are also discussed. MATLAB based simulation results are presented for the comparative study and analysis of DCMLI and conventional inverter (180 ^{0} & 120 ^{0}).

Index terms— Multi-level inverters, Diode Clamped Multi-level inverter, three-level DCMLI and Five-level DCMLI

1 INTRODUCTION

In recent years for higher power apparatus at megawatt levels multilevel inverters have become an attractive option because of better sinusoidal output voltage with lower dv/dt, less distortion and lower switching losses and frequency.

At high voltage levels (kv) it is difficult to connect a single power semiconductor switch directly to voltage grids, hence a new family of inverters is playing vital role at higher voltage levels. Basically multilevel inverters incorporate an array of power semiconductor devices such as IGBT and capacitor voltage sources, which generate a stepped output voltage. Based on the working principle, three topologies of multilevel inverters are reported in literature such as diode clamped multilevel inverter,Flying capacitor multilevel inverter, and cascaded H- Bridge multilevel inverter.

Fig.1 shows a schematic diagram of one-phase leg of inverters with different numbers of levels in which semiconductor is replaced by an ideal switch.Fig.1(a) shows an output voltage of two level with respect to negative terminal of capacitor, while Fig.1(b) shows three level output voltage. Fig.1(c) shows an output voltage of generalized n level. Let p is the number of steps of the phase voltage with respect to the negative terminal of the inverter, then the number of steps in the output voltage between two phases 'k' is given by eqn.(1)

$$k = 2m+1 \quad (1)$$

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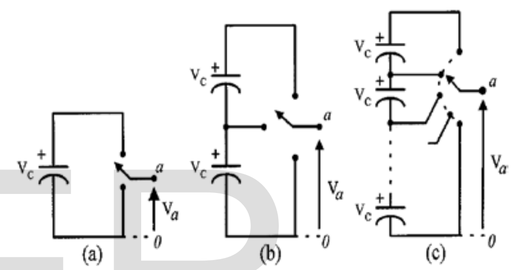

Fig1. Schematic diagram of one phase leg of inverter(a) two-level (b) three-level(c) n-level[1]

In this paper multi-level topology i.e Diode clamped multilevel inverter (three-level DCMLI and five-level DCMLI) is compared with conventional inverter (1800&1200) compared in terms of THD of the output voltage.

2 DIODE CLAMPED MULTI-LEVEL INVERTER

Fig.2 shows the single-phase five-level diode clamped multi-level inverter. The main concept of this inverter is to use diodes to limit the voltage stress of power devices [3]. The voltage over each capacitor and each switch is Vdc. An n level inverter needs (n-1) voltage sources, 2(n-1) switching devices and (n-1) (n-2) diodes.[2]

3 THREE-LEVEL DIODE CLAMPED MULTILEVEL INVERTER

It is basically a type of diode clamped multilevel inverter which gives output as its name suggests in three steps i.e +Vdc, 0, -Vdc. . In its circuit the dc bus voltage is split into three levels by two series capacitors. It differs from two level inverter in the way that the clamped diodes makes the switch voltage to half the level of the dc bus voltage.

4 FIVE-LEVEL DIODE CLAMPED MULTILEVEL INVERTER

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It is also one of the type of DCMLI in which the dc- bus consists of four capacitors. For dc-bus voltage Vdc, the voltage across each capacitor is Vdc/4 through clamping diodes. There are five switch combinations to synthesize five level voltages which is shown in Table no.2.

5 180 ^{0} CONVENTIONAL INVERTER

In the three phase inverter each SCR conducts for 1800 of a cycle thyristor pair. In each arm ,i.e. S1, S4; S3,S6 and S5, S2 are turned on with the time interval of 1800 it means that S1 conducts for 180o S4 for the next 1800 of a cycle thyristor in the upper group, i.e. S1, S3, S5 conduct at an interval of 1200.It implies that if S1 is fired at wt = to 0o then S3 must be fired at wt = 120oand S5 at wt = 2400. Same is true for lower group SCR's. We can also use IGBT or any other thyristor in place of SCR.

Table.1. Switching states for various voltages of a phase leg

Voltage level Vao=	S1	S2	S3	S4
Vdc/2	1	1	0	0
-Vdc/2	0	1	1	0
zero	0	0	1	1

Table.2. Switching states of five level multilevel inverter

V0	S1	S2	S3	S4	S5	S6	S7	S8
Vdc/2	1	1	1	1	0	0	0	0
Vdc/4	0	1	1	1	1	0	0	0
0	0	0	1	1	1	1	0	0
-Vdc/4	0	0	0	1	1	1	1	0
-Vdc/2	0	0	0	0	1	1	1	1

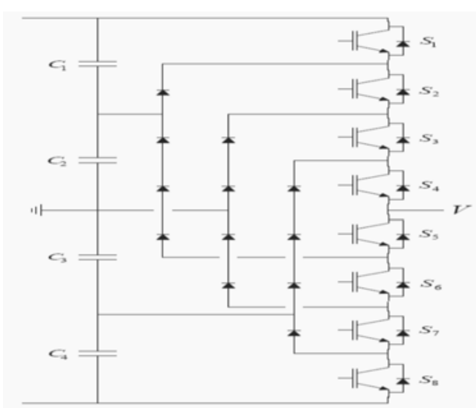

Fig.2. Single phase five-level diode clamped inverter[2]

6 120^0 CONVENTIONAL INVERTER

In this each thyristor conducts for 120^0 of a cycle. Like 180^0 mode, 120^0 mode inverter also requires six steps, each step of 60^0 duration, for completing one cycle of the output ac voltage. In this inverter too the sequence of firing the six thyristors is same the only difference is that 60^0 elapses between gating interval of one and commutation interval of second thyristor i.e. S1 conducts for 120^0 and 60^0 elapse occurs between gating of thyristor S3 and commutation of S1. Hence simulation model for both modes is same . They only differs in the pulse width provided.

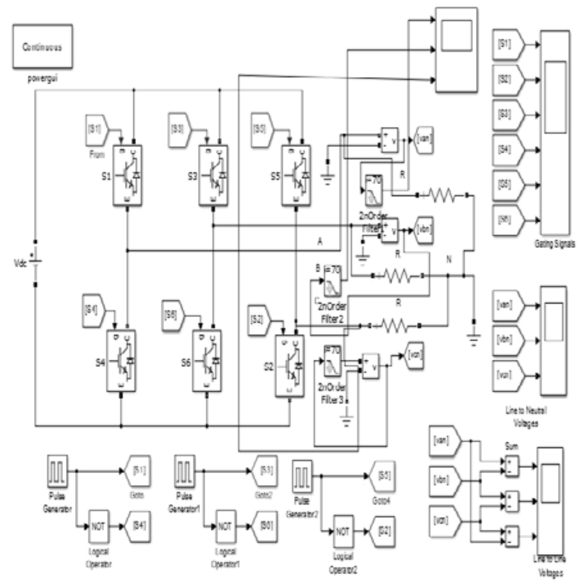

Fig.3. Simulation model of three phase 180^0 and 120^0 mode of conduction

7 RESULTS AND DISCUSSION

Simulation models of different multilevel inverter topologies are developed in MATLAB/Simulink environment. The parameter used for simulation study are given in Table No.3.

Table No.3

DC link parameters	
DC link voltage	300V
DC link capacitor	2200 µF
Filter parameter	
Cut off freq.	200Hz
Load parameters	
Rated line to line voltage	415 V
Load resistance	1 Ω
Frequency	50Hz

Phase voltage Vao and THD analysis of multilevel inverter topologies and conventional inverter are shown in figures . The waveforms of voltages are shown in figures without filtering and with filter.

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7.1 Performance of conventional inverter in 180^0 mode of conduction

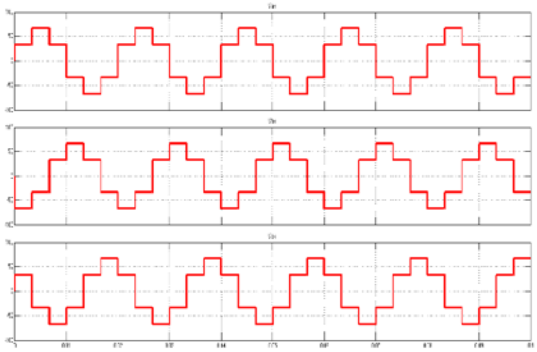

Fig.4. output voltages of conventional inverter (180^0) without filter

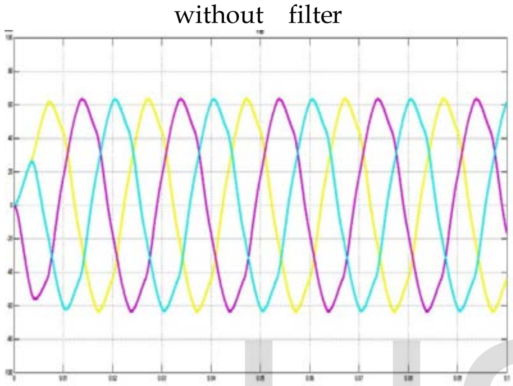

Fig.5. output voltages of conventional (180^0) inverter with filter

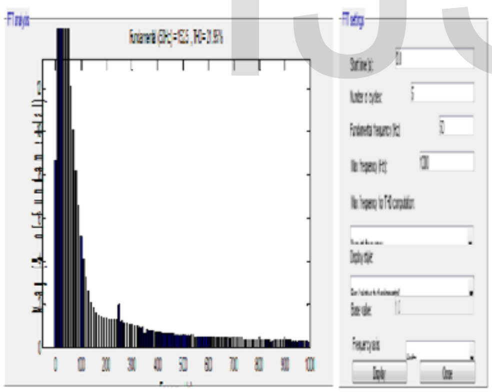

Fig.6.THD Analysis of conventional (180^0) inverter with filter i.e 21.95%

7.2 Performance of conventional inverter in 120^0 mode of conduction

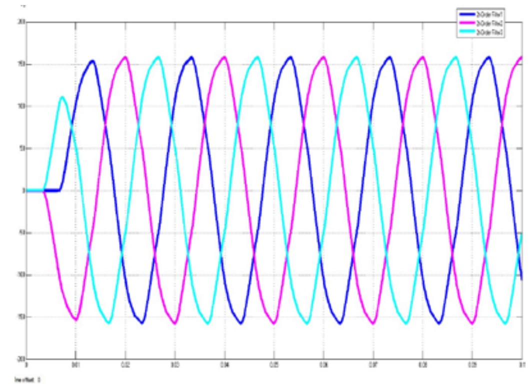

Fig.7. output voltage of conventional inverter (120^0) with Filter

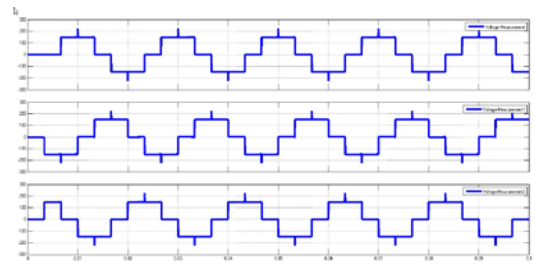

Fig.9. output voltage of conventional inverter (120^0) without filter

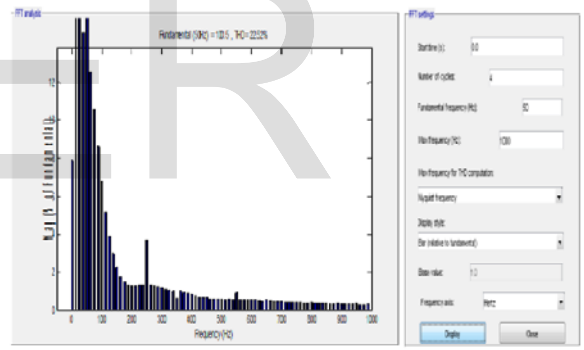

Fig.10. THD of conventional inverter (120^0) with filter i.e 22.52%

7.3 Performance of three phase five level DCMLI

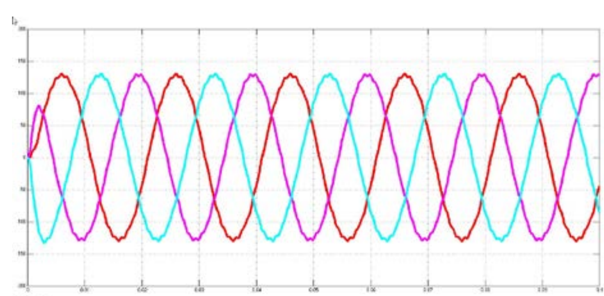

Fig.16. output voltage of three phase five level DCMLI with Filter

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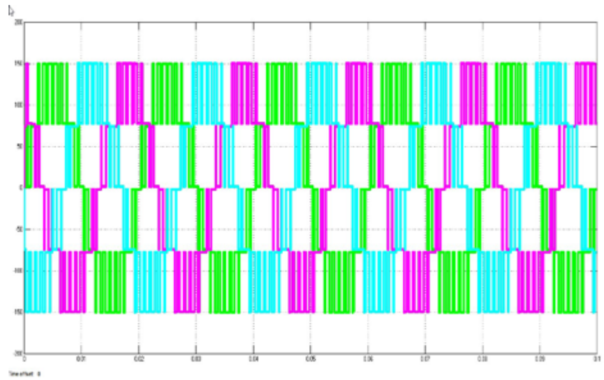

Fig.17. output voltage of three phase five level DCMLI without Filter

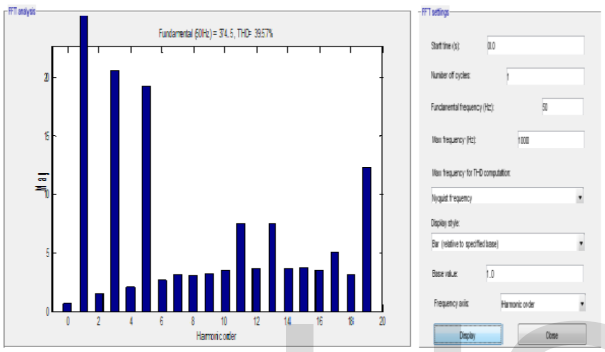

Fig.18. THD of three phase five level DCMLI with filter i.e 3.68%

7.4 Performance of three phase three level DCMLI

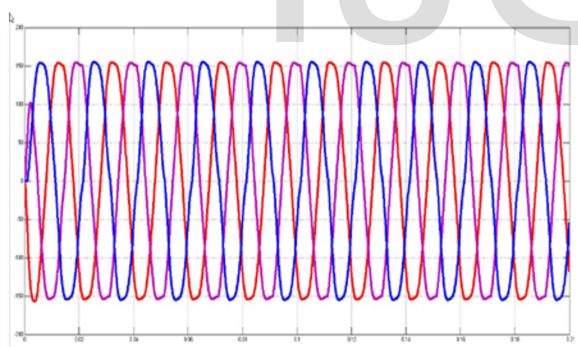

Fig.12.output voltage of three phase three level DCMLI without Filter

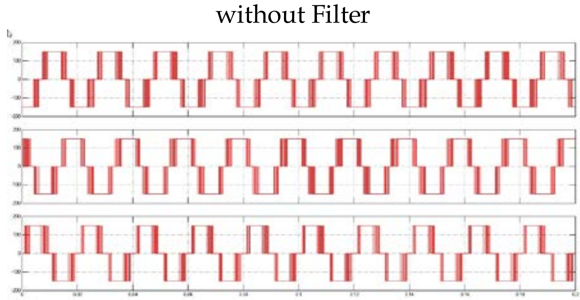

Fig.13. output voltage of three phase three level DCMLI without filter

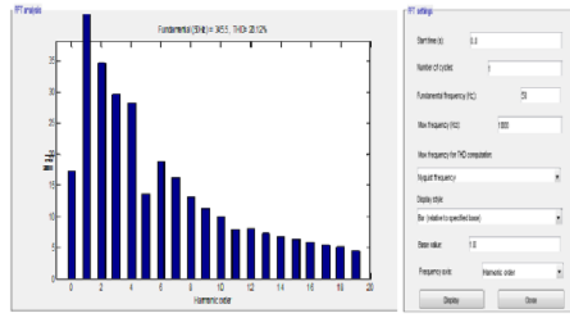

Fig.14. THD of three level DCMLI with filter i.e 20.12%

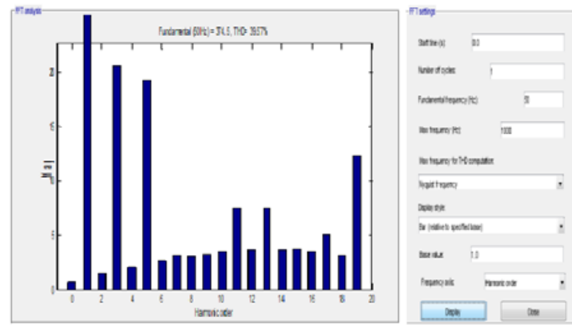

Fig.15. THD of three level DCMLI without Filter i.e 39.57%

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8 Control strategies PWM

PWM is a modulation technique that control the width of the rectangular pulse wave resulting in the variation of the average value of the waveform. PWM technique is the intersecting method which require sawtooth or rectangular wave as carrier signal and sinosuidal or rectangular as reference signal as shown in Fig, when the value of reference signal is more than the carrier signal the PWM signal is in high state otherwise it is in low state. The main advantage of PWM technique is that power loss in the switching devices is very low because when the switch is off there is practically no current and when switch is on then voltage drop across the switch is almost zero.

9 Comparison of THDs

Sr.no.	Inverter	THD
1.	Conventional inverter in 1800 mode of conduction filter	21.5%
2.	Conventional inverter in 1800 mode of conduction without filter	31.11%
3.	Conventional inverter in 1200 mode of conduction with filter	22.52%
4.	Conventional inverter in 1200 mode of conduction without filter	31.09%
5.	Three phase three level diode clamped multilevel inverter with filter	20.12%
6.	Three phase three level diode clamped multilevel inverter without filter	39.57%

7.	Three phase five level diode clamped multilevel inverter with filter	3.68%
8.	Three phase five level diode clamped multilevel inverter without filter	34.67%

XI.CONCLUSION

In this paper the conventional inverters (180^0 and 120^0) are studied and analyzed using simulation results in MATLAB/SIMULINK environment. The main focus of the work is to carried out a comparative analysis of conventional inverters with multilevel inverters in terms of THD (Total Harmonic Distortion) of their output voltages. For this comparative analysis different inverters topology are studied and diode clamped multilevel inverter is considered for the comparative analysis. As we know that in case of multilevel inverter the THD of the output voltage decreases with the increase in number of levels. Two types of diode clamped multilevel inverter (three level and five level) are modeled in MATLAB environment. From the various simulation results it is observed that five level multilevel diode clamped inverter is a better choice with THD as compared to other topologies studied in this paper.

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